NOIDA INSTITUTE OF ENGG. & TECHNOLOGY, GREATER NOIDA, GAUTAM BUDDH NAGAR
(AN AUTONOMOUS INSTITUTE)

Affiliated to

DR. A.P.J. ABDUL KALAM TECHNICAL UNIVERSITY UTTAR PRADESH, LUCKNOW

Evaluation Scheme & Syllabus

For

Master of Technology

VLSI Design

Second Year

(Effective from the Session: 2022-23)

NOIDA INSTITUTE OF ENGG. & TECHNOLOGY, GREATER NOIDA, GAUTAM BUDDH NAGAR
(AN AUTONOMOUS INSTITUTE)

Master of Technology
VLSI Design
EVALUATION SCHEME
SEMESTER -III

Sl. No.	Subject Codes	Subject	Periods			Evaluation Schemes				End Semester		Total	Credit
			L	T	P	CT	TA	TOTAL	PS	TE	PE		
1	AMTVL0351	Dissertation	0	0	30	-	-	-	200	-	300	500	15
2	AMTVL0352	Seminar-II	0	0	6	-	-	-	100	-	-	100	3
		GRAND TOTAL	0	0	36							600	18

Abbreviation Used:-
L: Lecture, T: Tutorial, P: Practical, CT: Class Test, TA: Teacher Assessment, PS: Practical Sessional, TE: Theory End Semester Exam., PE: Practical End Semester Exam.

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Master of Technology
VLSI Design
EVALUATION SCHEME
SEMESTER -IV

Sl. No.	Subject Codes	Subject	Periods			Evaluation Schemes				End Semester		Total	Credit
			L	T	P	CT	TA	TOTAL	PS	TE	PE		
1	AMTVL0451	Dissertation (Final)	0	0	36	-	-	-	200	-	400	600	18
		GRAND TOTAL	**0**	**0**	**36**							**600**	**18**

Abbreviation Used:-
L: Lecture, T: Tutorial, P: Practical, CT: Class Test, TA: Teacher Assessment, PS: Practical Sessional, TE: Theory End Semester Exam., PE: Practical End Semester Exam.